REVISIONS			
LTR	DESCRIPTION	DATE(YR-MO-DA)	APPROVED
A	Page 5, table I: change test condition for I_{IL} test. Pages 13, through 19, table III: change functions and descriptions for pins 25, 32, 38, 39, 56, 60, 62, and 74. Editorial changes throughout.	88-04-07	W. Heckman
B	Add device 02. Add vendor CAGE 88379. Add case outline Y (flat package). Editorial changes throughout. Change to reflect MIL-H-38534 processing.	90-04-13	W. Heckman
C	Made technical changes to table I. Add case outline Z (flat package). Editorial changes throughout.	92-02-18	G.A. Lude

REV	C	C	C	C	C	C	C	C	C	C										
SHEET	15	16	17	18	19	20	21	22	23	24										

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
87-08-06

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, DUAL REDUNDANT REMOTE TERMINAL UNIT (RTU), HYBRID

SIZE	CAGE CODE	
A	67268	5962-87535

SHEET 1 OF 24

DESC FORM 193
JUL 91

5962-E433

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class H hybrid microcircuits to be processed in accordance with MIL-H-38534.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-87535	01	X	X
Drawing number	Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish per MIL-H-38534

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	BUS-65112	Dual redundant remote terminal unit (RTU)
02	2452	Dual redundant remote terminal unit (RTU)

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	See figure 1 (78-lead, 1.870" x 2.100" x .250"), hybrid package
Y	See figure 1 (82-lead, 2.19" x 1.60" x .171"), flat package
Z	See figure 1 (82-lead, 2.19" x 1.60" x .200"), flat package

1.3 Absolute maximum ratings.

Logic supply voltage (V_L)	5.5 V dc
Positive supply voltage (V_{CC})	18.0 V dc
Negative supply voltage (V_{EE})	-18.0 V dc
Storage temperature range	-65°C to +150°C
Thermal rise, case to junction ($\triangle T_J$)	13.9°C
Lead soldering temperature (10 seconds)	+300°C
Power dissipation (T_C = +125°C)	Duty cycle dependent (see table I power supplies)

1.4 Recommended operating conditions.

Logic supply voltage (V_L)	+4.5 V dc to +5.5 V dc
Positive supply voltage (V_{CC})	+14.25 V dc to +15.75 V dc
Negative supply voltage (V_{EE})	-14.25 V dc to -15.75 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Maximum differential input voltage	40 Vp-p

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510	-	Microcircuits, General Specification for.
MIL-H-38534	-	Hybrid Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883	-	Test Methods and Procedures for Microelectronics.
MIL-STD-1553	-	Aircraft Internal Time Division Command/Response Multiplex Data Bus.

(Copies of the specifications and standards required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-H-38534 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-H-38534 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Pin functions. The pin functions shall be as specified in tables III and IV.

3.2.3 Block diagrams. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-H-38534. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in QML-38534 (see 6.6 herein).

3.6 Manufacturer eligibility. In addition to the general requirements of MIL-H-38534, the manufacturer of the part described herein shall submit for DESC-ECT review and approval electrical test data (variables format) on 22 devices from the initial quality conformance inspection group A lot sample, produced on the certified line, for each device type listed herein. The data should also include a summary of all parameters manually tested, and for those which, if any, are guaranteed.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Receiver							
Differential input impedance	Z_{IN} diff	DC to 1 MHz	2/	All	4		kΩ
Differential input voltage	V_{IN} diff		2/	All		40	Vp-p
Input threshold	V_{TH}	Direct coupled (across 35Ω load)	4,5,6	All		1.2	Vp-p
Common mode rejection ratio	CMRR	DC to 2 MHz	2/ 3/	All	40		dB
Common mode voltage	CMV	DC to 2 MHz	2/ 3/	All	-10	+10	V
Transmitter							
Differential output voltage	V_{OUT} diff	Direct coupled (across 35Ω load)	4,5,6	All	6.0	9.0	Vp-p
Output rise and fall time	t_r, t_f		9,10,11	01	100	180	ns
			9,10,11	02	100	300	ns
Output noise	N_{OUT}		2/ 3/	All		14	mVp-p
Logic							
High level input voltage	V_{IH}	V_L = 5.5 V	1,2,3	All	2.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level input voltage	V_{IL}	V_L = 5.5 V	1,2,3	All		0.7	V
High level input current 4/	I_{IH}	V_L = 5.5 V V_{IH} = 2.7 V	1,2,3	All	-0.7	-0.03	mA
High level input current 5/	I_{IH}	V_L = 5.5 V V_{IH} = 2.7 V	1,2,3	01	-20	+20	µA
				02	-300	+20	
Low level input current 4/	I_{IL}	V_L = 5.5 V V_{IL} = 0.4 V	1,2,3	01	-1.6	-.09	mA
				02	-1.6	+.02	
Low level input current 5/	I_{IL}	V_{IL} = 0.4 V	1,2,3	01	-20	+20	µA
				02	-300	+20	
High level output voltage 6/	V_{OH}	V_L = 4.5 V I_{OH} = 0.3 mA	1,2,3	All	2.7		V
High level output voltage 7/	V_{OH}	V_L = 4.5 V I_{OH} = 3 mA	1,2,3	All	2.7		V
Low level output voltage 8/	V_{OL}	V_L = 4.5 V I_{OH} = -1.6 mA	1,2,3	All		0.4	V
Low level output voltage 9/	V_{OL}	V_L = 4.5 V I_{OH} = -4 mA	1,2,3	All		0.4	V
Low level output voltage 7/	V_{OL}	V_L = 4.5 V I_{OH} = -6 mA	1,2,3	All		0.4	V
Functional test 10/			7,8	All			pass/ fail
Input capacitance	C_I	f = 1 MHz	See 4.3.1c	All		50	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input/output capacitance 7/	C_{IO}	f = 1 MHz	See 4.3.1c	All		50	pF
Power supplies							
+5 V dc current drain	I_L	V_L = 5.5 V dc Inputs = 0 V dc, except 12 MHz Clock input active All outputs open	1,2,3	All		160	mA
-15 V dc current drain	I_{EE}	V_{EE} = -15.75 V dc	1,2,3	All		60	mA
+15 V dc current drain	I_{CC}	V_{CC} = +15.75 V dc					
- idle			1,2,3	All		80	mA
- 25% transmit			1,2,3	All		130	mA
- 50% transmit			1,2,3	All		180	mA
- 100% transmit			1,2,3	All		280	mA

1/ V_{CC} = +15 V, V_{EE} = -15 V, V_L = +5 V unless otherwise specified.

2/ This parameter is not tested, but is guaranteed by design.

3/ Receiver and transmitter parameters are specified with transformer.

4/ I_{IH} and I_{IL} for input pins BRO ENA, ADDRE, ADDRC, ADDRA, ADDRD, ADDRB, and ADDRP. (These inputs have internal pull up resistors connected.)

5/ I_{IH} and I_{IL} for all input pins other than in note 4.

6/ V_{OH} for all output pins other than in note 7.

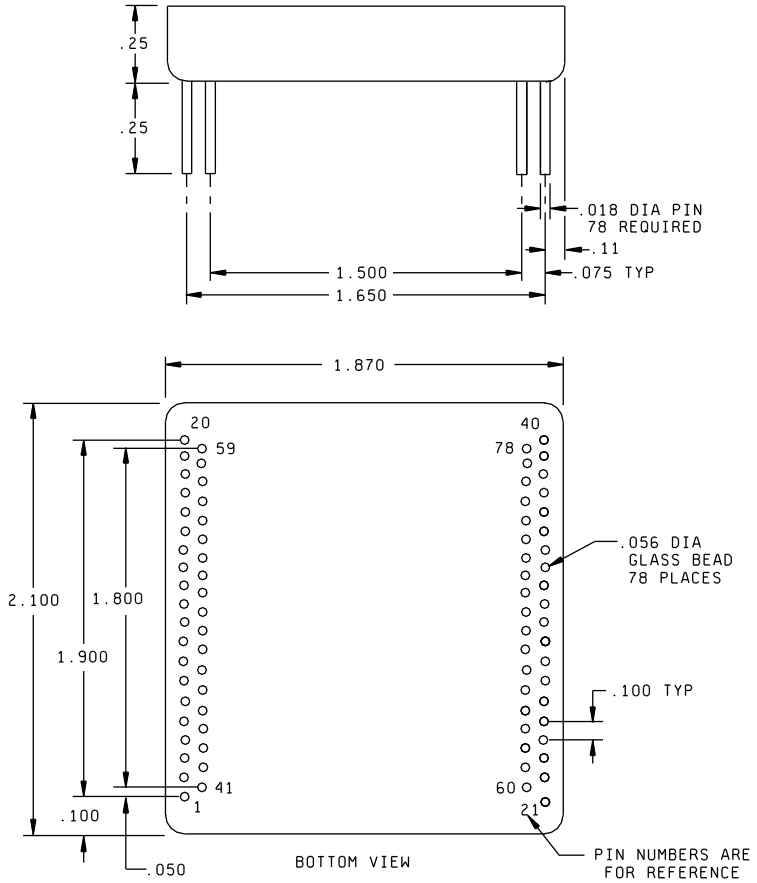
7/ V_{OL}, V_{OH}, and C_{IO} for pins DB0 through DB15.

8/ V_{OL} for output pins A10, A8, A6, $\overline{\text{HSFAIL}}$, A5, $\overline{\text{RTFAIL}}$, A11, $\overline{\text{BITEN}}$, $\overline{\text{NBGT}}$, A9, A7, $\overline{\text{GBR}}$, $\overline{\text{ME}}$, STATEN.

9/ V_{OL} for output pins $\overline{\text{RTADERR}}$, A3, A1, INCMD, $\overline{\text{DTSTR}}$, $\overline{\text{DTREQ}}$, A2, A0, $\overline{\text{DTACK}}$, A4, R/$\overline{\text{W}}$.

10/ Functional tests performed to verify functionally to MIL-STD-1553 RTU protocol.

CASE X



Inches	mm
.018	0.45
.050	1.27
.056	1.42
.075	1.91
.100	2.54
.11	2.8
.25	6.4
1.500	38.10
1.650	41.91
1.800	45.72
1.870	47.50
1.900	48.26
2.100	53.34

FIGURE 1. Case outlines.

CASE Y

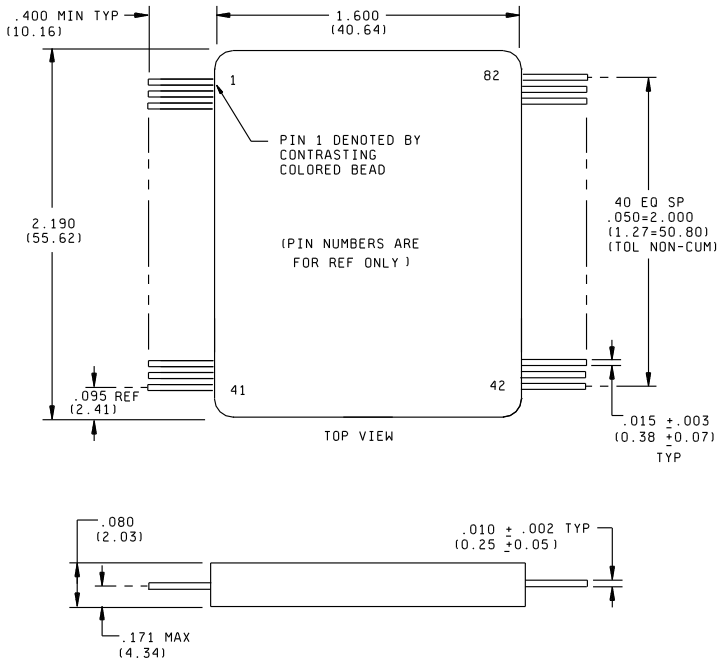
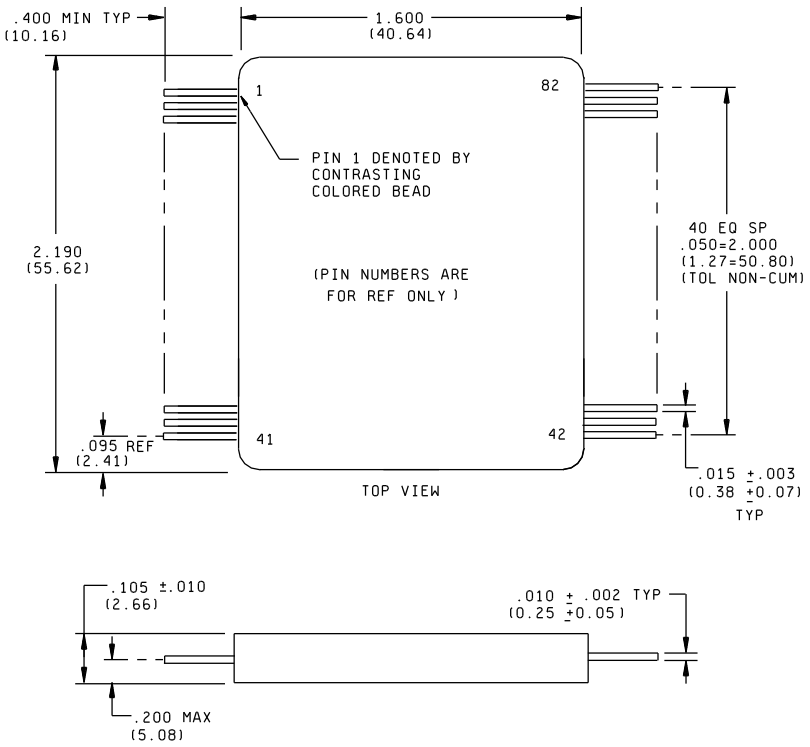


FIGURE 1. Case outlines - Continued.

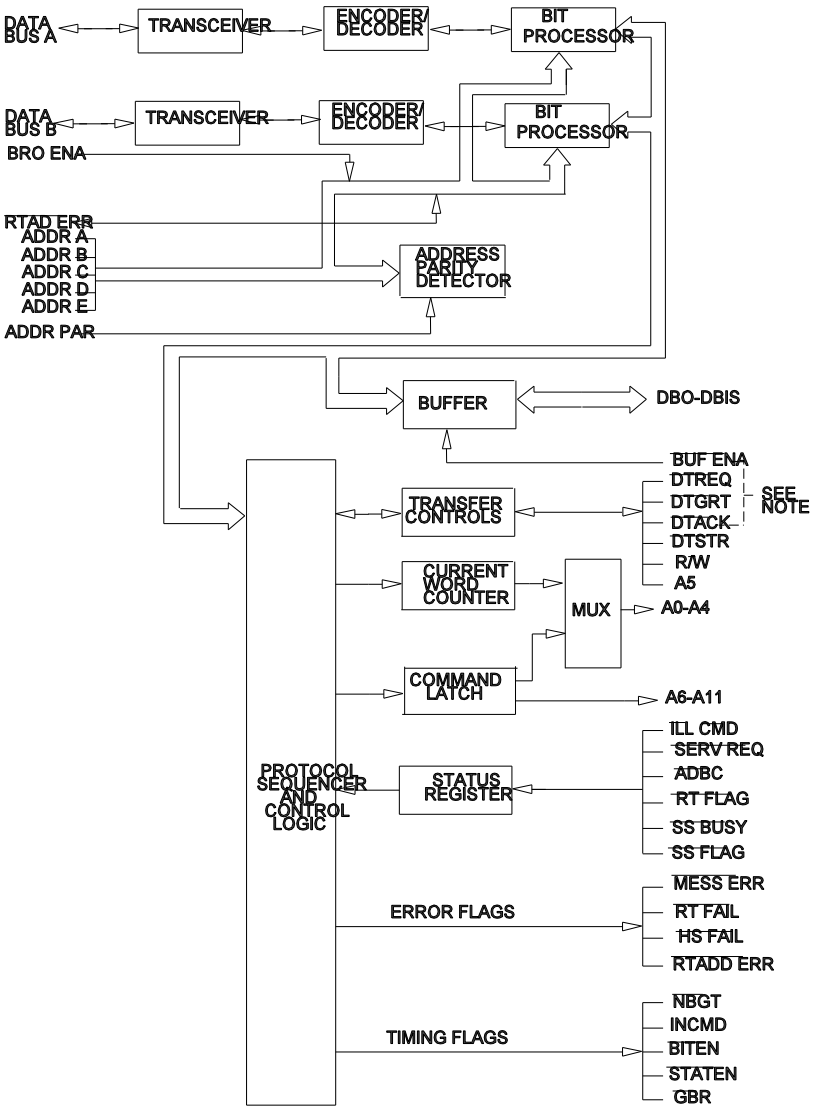
CASE Z



NOTES:

1. **Dimensions are in inches.**
2. **Metric equivalents are given for general information only.**
3. **Unless otherwise specified, tolerance is ±0.005 (0.13 mm) for three place decimals and ±0.1 (0.25 mm)for two place decimals.**
4. **Case Z is a conductive package.**

FIGURE 1. Case outlines - Continued.



NOTE: For most user applications, $\overline{\text{DTACK}}$ can be connected directly to $\overline{\text{BUF ENA}}$.

FIGURE 2. Block diagram.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in QML-38534 (see 6.6 herein). The certificate of compliance submitted to DESC-ECT prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-H-38534 and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-H-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-H-38534.

4.2 Screening. Screening shall be in accordance with MIL-H-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.7 herein).

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-H-38534 and as specified herein.

4.3.1 Group A inspection. Group A inspection shall be in accordance with MIL-H-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 shall be omitted.

c. Subgroup 4 (C_I and C_{IO} measurement) shall be measured only for the initial test and after process or design changes which may affect input and output capacitance.

4.3.2 Group B inspection. Group B inspection shall be in accordance with MIL-H-38534.

4.3.3 Group C inspection. Group C inspection shall be in accordance with MIL-H-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.7 herein).

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection. Group D inspection shall be in accordance with MIL-H-38534.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5008, group A test table)
Interim electrical parameters	1, 4, 7, 9
Final electrical test parameters	1*,2,3,4,5,6,9,10,11
Group A test requirements	1,2,3,4,5,6,9,10,11
Group C end-point electrical parameters	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-H-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for original equipment design applications and logistic support of existing equipment.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECT, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-ECT, Dayton, Ohio 45444, or telephone (513) 296-5374.

6.6 Approved sources of supply. Approved sources of supply are listed in QML-38534. Additional sources will be added to QML-38534 as they become available. The vendors listed in QML-38534 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DESC-ECT.

TABLE III. Pin function, case X (dual-in-line).

Pin	Function	Description
1	A10	Latched output of the most significant bit (MSB) in the subaddress field of the command word.
2	A8	Latched output of the third most significant bit in the subaddress field of the command word.
3	A6	latched output of the least significant bit (LSB) in the subaddress field of the command word.
4	DB1	Bidirectional parallel data bus bit 1.
5	DB3	Bidirectional parallel data bus bit 3.
6	DB5	Bidirectional parallel data bus bit 5.
7	DB7	Bidirectional parallel data bus bit 7.
8	DB9	Bidirectional parallel data bus bit 9.
9	DB11	Bidirectional parallel data bus bit 11.
10	DB13	Bidirectional parallel data bus bit 13.
11	DB15	Bidirectional parallel data bus bit 15 (MSB).
12	BRO ENA	Broadcast enable - When HIGH, this input allows recognition of an RT address of all ones in the command word as a broadcast message. When LOW, it prevents response to RT address 31 unless it was the assigned terminal address.
13	ADDRE	Input of the MSB of the assigned terminal address.
14	ADDRC	Input of the 3rd MSB of the assigned terminal address.
15	ADDRA	Input of the LSB of the assigned terminal address.
16	$\overline{\text{RTADERR}}$	Output signal used to inform subsystem of an address parity error. If LOW, indicates parity error and the RT will not respond to any command address to a single terminal. It will respond to broadcast commands if BRO ENA is HIGH.
17	$\overline{\text{TXDATAOUT B}}$	LOW output to the primary side of the coupling transformer that connects to the B channel of the 1553 bus.
18	V_{CC} B	+15 volt input power supply connection for the B channel transceiver.
19	GND B	Power supply return connection for the B channel transceiver.
20	RXDATA	Input from the HIGH side of the primary side of the coupling transformer that connects to the B channel of the 1553 bus.

TABLE III. Pin function, case X (dual-in-line) - Continued.

Pin	Function	Description
21	A3	Multiplexed address line output. When INCMD is LOW, or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the 2nd MSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the 2nd MSB of the current word counter.
22	A1	Multiplexed address line output. When INCMD is LOW, or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the 2nd LSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter.
23	$\overline{\text{DTGRT}}$	Data transfer grant - Active LOW input signal from the subsystem that informs the RT, when DTREQ is asserted, to start the transfer. Once the transfer is started, DTGRT can be removed.
24	INCMD	In command - HIGH level output signal used to inform the subsystem that the RT is presently servicing a command. When low, A0-A4 represent the word count of the present command. When high, A0-A4 represent the current word counter of non-mode commands.
25	$\overline{\text{HSFAIL}}$	Handshake fail - Output signal that goes LOW and stays LOW whenever the subsystem fails to supply DTGRT in time to do a successful transfer. Cleared by the next NBGT.
26	$\overline{\text{DTSTR}}$	DATA strobe - A LOW level output pulse (166 ns) present in the middle of every data word transfer over the parallel data bus. Used to latch or strobe the data into memory, FIFOs, registers, etc. Recommend using the rising edge to clock data in.
27	A5	Address line output that is LOW whenever the command word is being transferred to the subsystem over the parallel data bus, and is HIGH whenever data words are being transferred.
28	$\overline{\text{RTFAIL}}$	Remote terminal failure - latched active LOW output signal to the subsystem to flag detection of a remote terminal continuous self-test failure. Cleared by the start of the next message transmission (status word) and set if problem is again detected.
29	$\overline{\text{DTREQ}}$	Data transfer request - Active LOW output signal to the subsystem indicating that the RT has data for or needs data from the subsystem and requests a data transfer over the parallel data bus. Will stay LOW until transfer is completed or transfer timeout has occurred.

TABLE III. Pin function, case X (dual-in-line) - Continued.

Pin	Function	Description
30	$\overline{\text{ADBC}}$	Accept dynamic bus control - Active LOW input signal from subsystem used to set the dynamic bus control acceptance bit in the status register if the command word was a valid, legal mode command for dynamic bus control.
31	TEST 2	Factory test point - DO NOT USE.
32	A11	Latched output of the T/$\overline{\text{R}}$ bit in the command word.
33	$\overline{\text{ILLCMD}}$	Illegal command - Active LOW input signal from the subsystem, strobes in on the rising edge of INCMD. Used to define the command word as illegal and to set the message error bit in the status register.
34	$\overline{\text{SRQ}}$	Subsystem service request - Input from the subsystem used to control the service request bit in the status register. If LOW when the status word is updated, the service request bit will be set; if HIGH, it will be cleared.
35	$\overline{\text{BITEN}}$	Built-in-test word enable - LOW level output pulse (.5 µs), present when the built-in-test word is enabled on the parallel data bus.
36	$\overline{\text{RXDATAIN A}}$	Input from the LOW side of the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
37	V_L A	+5 Volt input power supply connection for the A channel transceiver.
38	V_{EE} A	-15 volt input power supply connection for the A channel transceiver.
39	$\overline{\text{TXDATAOUT A}}$	HIGH output to the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
40	$\overline{\text{NBGT}}$	New bus grant - LOW level output pulse (166 ns) used to indicate the start of a new protocol sequence in response to the command word just received.
41	A9	Latched output of the 2nd MSB in the subaddress field of the command word.
42	A7	Latched output of the 2nd LSB in the subaddress field of the command word.
43	DB0	Bidirectional parallel data bus bit 0 (LSB).
44	DB2	Bidirectional parallel data bus bit 2.
45	DB4	Bidirectional parallel data bus bit 4.
46	DB6	Bidirectional parallel data bus bit 6.

TABLE III. Pin function, case X (dual-in-line) - Continued.

Pin	Function	Description
47	DB8	Bidirectional parallel data bus bit 8.
48	DB10	Bidirectional parallel data bus bit 10.
49	DB12	Bidirectional parallel data bus bit 12.
50	DB14	Bidirectional parallel data bus bit 14.
51	V_L	+5 volt input power supply connection for RTU digital logic section.
52	GND	Power supply return for RTU digital logic section.
53	ADDRD	Input of the 2nd MSB of the assigned terminal address.
54	ADDRB	Input of the 2nd LSB of the assigned terminal address.
55	ADDRP	Input of address parity bit. The combination of assigned terminal address and ADDRP must be odd parity for the RT to work.
56	TXDATAOUT B	HIGH, output to the primary side of the coupling transformer that connects to the B channel of the 1553 bus.
57	V_{EE} B	-15 volt input power supply connection for the B channel transceiver.
58	V_L B	+5 volt input power supply connection for the B channel transceiver.
59	$\overline{\text{RXDATAIN B}}$	Input from the LOW side of primary side of the coupling transformer that connects to the B channel of the 1553 bus.
60	A2	Multiplexed address line output. When INCMD is LOW, or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the 3rd MSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the 3rd MSB of the current word counter.
61	A0	Multiplexed address line output. When INCMD is LOW, or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the MSB in the word count field of the command. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the LSB of the current word counter.

TABLE III. Pin function, case X (dual-in-line) - Continued.

Pin	Function	Description
62	$\overline{\text{DTACK}}$	Data transfer acknowledge - Active LOW output signal during data transfers to or from the subsystem indicating the RTU has received the DTGRT in response to DTREQ and is presently doing the transfer. Can be connected directly to pin 67 (BUF ENA) for control of tri-state data buffers; and to tri-state address buffer control lines, if they are used.
63	A4	Multiplexed address line output. When INCMD is LOW or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the MSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the MSB of the current word counter.
64	R/$\overline{\text{W}}$	Read/$\overline{\text{Write}}$ - Output signal that controls the direction of the internal data bus buffers. Normally, the signal is LOW and the buffers drive the data bus. When data is needed from the subsystem, it goes HIGH to turn the buffers around and the RT now appears as an input. The signal is HIGH only when DTREQ is active (LOW).
65	$\overline{\text{GBR}}$	Good block received - LOW level output pulse (.5 µs) used to flag the subsystem that a valid, legal, non-mode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem.
66	12 MHz IN	12 MHz clock input - Input for the master clock used to run RTU circuits.
67	$\overline{\text{BUF ENA}}$	Buffer enable - Input used to enable or 3-state the internal data bus buffers when they are driving the bus. When LOW, the data bus buffers are enabled. Could be connected to DTACK (pin 62) if RT is sharing the same data bus as the subsystem.
68	$\overline{\text{RESET}}$	Input resets entire RT when LOW.
69	$\overline{\text{RTFLAG}}$	Remote terminal flag - Input signal used to control the terminal flag bit in the status register. If LOW when the status word is updated, the terminal flag bit would be set; if HIGH, it would be cleared. Normally connected to RTFAIL (pin 28).
70	TEST 1	Factory test point - DO NOT USE.

TABLE III. Pin function, case X (dual-in-line) - Continued.

Pin	Function	Description
71 (device 01 only)	$\overline{\text{BUSY}}$	Subsystem busy - Input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set; if HIGH, it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands, data will still be transferred to subsystem.
71 (device 02 only)	$\overline{\text{BUSY}}$	Subsystem busy - Input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set; if HIGH, it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command.
72	$\overline{\text{SSFLAG}}$	Subsystem flag - Input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated, the subsystem flag will be set; if HIGH, it will be cleared.
73	$\overline{\text{ME}}$	Message error - Output signal that goes LOW and stays low whenever there is a format or word error with the received message over the 1553 data bus. Cleared by the next NBGT.
74	RXDATAIN A	Input from the HIGH side of the primary side of the coupling transformer that contacts to the A channel of the 1553 bus.
75	GNDA	Power supply return connection for the A channel transceiver.
76	V_{CC} A	+15 volt input power supply connection for the A channel transceiver.
77	$\overline{\text{TXDATAOUT A}}$	LOW output to the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
78	$\overline{\text{STATEN}}$	Status word enable - LOW level active output signal present when the status word is enabled on the parallel data bus.

TABLE IV. Pin function, cases Y and Z (flat package).

Pin	Function	Description
1	NC	No connection
2	A10	Latched output of the most significant bit (MSB) in the subaddress field of the command word.
3	A9	Latched output of the 2nd MSB in the subaddress field of the command word.
4	A8	Latched output of the third most significant bit in the subaddress field of the command word.
5	A7	Latched output of the 2nd LSB in the subaddress field of the command word.
6	A6	Latched output of the least significant bit (LSB) in the subaddress field of the command word.
7	DB0	Bidirectional parallel data bus bit 0 (LSB).
8	DB1	Bidirectional parallel data bus bit 1.
9	DB2	Bidirectional parallel data bus bit 2.
10	DB3	Bidirectional parallel data bus bit 3.
11	DB4	Bidirectional parallel data bus bit 4.
12	DB5	Bidirectional parallel data bus bit 5.
13	DB6	Bidirectional parallel data bus bit 6.
14	DB7	Bidirectional parallel data bus bit 7.
15	DB8	Bidirectional parallel data bus bit 8.
16	DB9	Bidirectional parallel data bus bit 9.
17	DB10	Bidirectional parallel data bus bit 10.
18	DB11	Bidirectional parallel data bus bit 11.
19	DB12	Bidirectional parallel data bus bit 12.
20	DB13	Bidirectional parallel data bus bit 13.
21	DB14	Bidirectional parallel data bus bit 14.
22	DB15	Bidirectional parallel data bus bit 15 (MSB).
23	V_L	+5 volt input power supply connection for RTU digital logic section.
24	BRO ENA	Broadcast enable - When HIGH, this input allows recognition of an RT address of all ones in the command word as a broadcast message. When LOW, it prevents response to RT address 31 unless it was the assigned terminal address.

TABLE IV. Pin function, cases Y and Z (flat package) - Continued.

Pin	Function	Description
25	GND	Power supply return for RTU digital logic section.
26	ADDRE	Input of the MSB of the assigned terminal address.
27	ADDRD	Input of the 2nd MSB of the assigned terminal address.
28	ADDRC	Input of the 3rd MSB of the assigned terminal address.
29	ADDRB	Input of the 2nd LSB of the assigned terminal address.
30	ADDRA	Input of the LSB of the assigned terminal address.
31	ADDRP	Input of address parity bit. The combination of assigned terminal address and ADDRP must be odd parity for the RT to work.
32	$\overline{\text{RTADERR}}$	Output signal used to inform subsystem of an address parity error. If LOW, indicates parity error and the RT will not respond to any command address to a single terminal. It will respond to broadcast commands if BRO ENA is HIGH.
33	TXDATAOUT B	HIGH output to the primary side of the coupling transformer that connects to the B channel of the 1553 bus.
34	$\overline{\text{TXDATAOUT B}}$	LOW output to the primary side of the coupling transformer that connects to the B channel of the 1553 bus.
35	V_{EE} B	-15 volt input power supply connection for the B channel transceiver.
36	V_{CC} B	+15 volt input power supply connection for the B channel transceiver.
37	V_L B	+5 volt input power supply connection for the B channel transceiver.
38	GND B	Power supply return connection for the B channel transceiver.
39	$\overline{\text{RXDATAIN B}}$	Input from the LOW side of primary side of the coupling transformer that connects to the B channel of the 1553 bus.
40	RXDATAIN B	Input from the HIGH side of the primary side of the coupling transformer that connects to the B channel of the 1553 bus.
41	NC	No connection
42	NC	No connection

TABLE IV. Pin function, cases Y and Z (flat package) - Continued.

Pin	Function	Description
43	$\overline{\text{NBGT}}$	New bus grant - LOW level output pulse (166 ns) used to indicate the start of a new protocol sequence in response to the command word just received.
44	$\overline{\text{STATEN}}$	Status word enable - LOW level active output signal present when the status word is enabled on the parallel data bus.
45	TXDATAOUT A	HIGH output to the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
46	$\overline{\text{TXDATAOUT A}}$	LOW output to the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
47	V_{EE} A	-15 volt input power supply connection for the A channel transceiver.
48	V_{CC} A	+15 volt input power supply connection for the A channel transceiver.
49	V_L A	+5 volt input power supply connection for the A channel transceiver.
50	GNDA	Power supply return connection for the A channel transceiver.
51	$\overline{\text{RXDATAIN A}}$	Input from the LOW side of the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
52	RXDATA A	Input from the HIGH side of the primary side of the coupling transformer that connects to the A channel of the 1553 bus.
53	$\overline{\text{BITEN}}$	Built-in-test word enable - LOW level output pulse (.5 µs), present when the built-in-test word is enabled on the parallel data bus.
54	$\overline{\text{ME}}$	Message error - Output signal that goes LOW and stays low whenever there is a format or word error with the received message over the 1553 data bus. Cleared by the next NBGT.
55	$\overline{\text{SRQ}}$	Subsystem service request - Input from the subsystem used to control the service request bit in the status register. If LOW when the status word is updated, the service request bit will be set; if HIGH, it will be cleared.
56	$\overline{\text{SSFLAG}}$	Subsystem flag - Input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated, the subsystem flag will be set; if HIGH, it will be cleared.

TABLE IV. Pin function, cases Y and Z (flat package) - Continued.

Pin	Function	Description
57	$\overline{\text{ILLCMD}}$	Illegal command - Active LOW input signal from the subsystem, strobes in on the rising edge of INCMD. Used to define the command word as illegal and to set the message error bit in the status register.
58 (device 01 only)	$\overline{\text{BUSY}}$	Subsystem busy - Input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set; if HIGH, it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands, data will still be transferred to subsystem.
58 (device 02 only)	$\overline{\text{BUSY}}$	Subsystem busy - Input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set; if HIGH, it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command.
59	A11	Latched output of the $\overline{\text{T}}$/R bit in the command word.
60	TEST 1	Factory test point - DO NOT USE.
61	TEST 2	Factory test point - DO NOT USE.
62	$\overline{\text{RTFLAG}}$	Remote terminal flag - Input signal used to control the terminal flag bit in the status register. If LOW when the status word is updated, the terminal flag bit would be set; if HIGH, it would be cleared. Normally connected to RTFAIL (pin 28).
63	$\overline{\text{ADBC}}$	Accept dynamic bus control - Active LOW input signal from subsystem used to set the dynamic bus control acceptance bit in the status register if the command word was a valid, legal mode command for dynamic bus control.
64	$\overline{\text{RESET}}$	Input resets entire RT when LOW.
65	$\overline{\text{DTREQ}}$	Data transfer request - Active LOW output signal to the subsystem indicating that the RT has data for or needs data from the subsystem and requests a data transfer over the parallel data bus. Will stay LOW until transfer is completed or transfer timeout has occurred.
66	$\overline{\text{BUF ENA}}$	Buffer enable - Input used to enable or 3-state the internal data bus buffers when they are driving the bus. When LOW, the data bus buffers are enabled. Could be connected to DTACK (pin 62) if RT is sharing the same data bus as the subsystem.

TABLE IV. Pin function, cases Y and Z (flat package) - Continued.

Pin	Function	Description
67	$\overline{\text{RTFAIL}}$	Remote terminal failure - Latched active LOW output signal to the subsystem to flag detection of a remote terminal continuous self-test failure. Cleared by the start of the next message transmission (status word) and set if problem is again detected.
68	12 MHz IN	12 MHz clock input - Input for the master clock used to run RTU circuits.
69	A5	Address line output that is LOW whenever the command word is being transferred to the subsystem over the parallel data bus, and is HIGH whenever data words are being transferred.
70	$\overline{\text{GBR}}$	Good block received - LOW level output pulse (.5 µs) used to flag the subsystem that a valid, legal, non-mode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem.
71	$\overline{\text{DTSTR}}$	DATA strobe - A LOW level output pulse (166 ns) present in the middle of every data word transfer over the parallel data bus. Used to latch or strobe the data into memory, FIFOs, registers, etc. Recommend using the rising edge to clock data in.
72	R/$\overline{\text{W}}$	Read/$\overline{\text{Write}}$ - Output signal that controls the direction of the internal data bus buffers. Normally, the signal is LOW and the buffers drive the data bus. When data is needed from the subsystem, it goes HIGH to turn the buffers around and the RT now appears as an input. The signal is HIGH only when DTREQ is active (LOW).
73	$\overline{\text{HSFAIL}}$	Handshake fail - Output signal that goes LOW and stays LOW whenever the subsystem fails to supply DTGRT in time to do a successful transfer. Cleared by the next NBGT.
74	A4	Multiplexed address line output. When INCMD is LOW or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the MSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the MSB of the current word counter.
75	INCMD	In command - HIGH level output signal used to inform the subsystem that the RT is presently servicing a command. When low, A0-A4 represent the word count of the present command. When high, A0-A4 represent the current word counter of non-mode commands.

TABLE IV. Pin function, cases Y and Z (flat package) - Continued.

Pin	Function	Description
76	$\overline{\text{DTACK}}$	Data transfer acknowledge - Active LOW output signal during data transfers to or from the subsystem indicating the RTU has received the DTGRT in response to DTREQ and is presently doing the transfer. Can be connected directly to pin 67 (BUF ENA) for control of 3-state data buffers; and to tri-state address buffer control lines, if they are used.
77	$\overline{\text{DTGRT}}$	Data transfer grant - Active LOW input signal from the subsystem that informs the RT, when DTREQ is asserted, to start the transfer. Once the transfer is started, DTGRT can be removed.
78	A0	Multiplexed address line output. When INCMD is LOW or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the LSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the LSB of the current word counter.
79	A1	Multiplexed address line output. When INCMD is LOW or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the 2nd LSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter.
80	A2	Multiplexed address line output. When INCMD is LOW or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the 3rd MSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the 3rd MSB of the current word counter.
81	A3	Multiplexed address line output. When INCMD is LOW or A6 through A10 are all zeroes or all ones (mode command), it represents the latched output of the 2nd MSB in the word count field of the command word. When INCMD is HIGH and A6 through A10 are not all zeroes or all ones, it represents the 2nd MSB of the current word counter.
82	NC	No connection

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 92-02-18

Approved sources of supply for SMD 5962-87535 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EL. This bulletin is superseded by the next dated revision of QML-38534.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8753501XX	19645	BUS-65112
5962-8753501YX	19645	BUS-65117
5962-8753502XX	19645	ARX2542
5962-8753502YX	19645	ARX2542FP

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
50821	ILC Data Device Corporation 105 Wilbur Place Bohemia, NY 11716
88379	Aeroflex Laboratories, Incorporated 35 South Service Road Plainview, NY 11803